UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,699	02/14/2002	Sandor T. Farkas	016295.0768	8818

7590 01/04/2005

Michael A. Hawes
Baker Botts, L.L.P.
One Shell Plaza
910 Louisiana Street
Houston, TX 77002-4995

EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,699	FARKAS ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/14/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lovett (US Patent no 6,097,222) in view of Wigley et al (US Patent no 4,187,535).

4. As per claims 1, 10 and 20, Lovett discloses

A power supply having a positive remote sense input [inherent as conventional computer power supplies include a remote sense connection, including both a positive and negative input];

a pull-down circuit having at least two inputs and an output [col. 15, lines 52-56; col. 16, lines 5-10; detail description of Fig. 10, 14, 16, 18].

Lovett discloses the details of the pull-down circuit in respect to a NOR gate where the pull-down circuit provides a substantially uniform or symmetrical high-to-low output slew rate

regardless of the order in which inputs transition from a low state to a high state. Lovett does not expressly disclose the invention in respect to a power supply. However, Wigley et al expressly disclose the use of a pull-up and pull-down circuit arrangement to provide an adjustable output voltage having an amplitude not exceeding the amplitude of the drive voltage [col. 2, lines 40-45; col. 15, line 51-- col. 16, line 4; col. 18, lines 23-26]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as one details the structure of the pull-down circuit and another discloses the use of the pull-down circuit to produce adjustable output voltage. Moreover, both Lovett and Wigley et al clearly recognize the advantage of using a pull-down circuit to output a voltage that is not greater than either of two input/drive voltages.

5. As per claims 2 and 11, Lovett and Wigley et al disclose that the output voltage is within 1% of the lesser of the input/drive voltages [Lovett: col. 7, lines 37-40; Wigley et al: col. 2, lines 40-45].

6. As per claims 3 and 12, Lovett discloses that the first load position includes a plurality of expansion connectors adapted to receive expansion cards [inherent to a computer system].

7. As per claims 4 and 13, Lovett discloses that the second load position includes a SCSI connector capable of coupling a plurality of SCSI devices [well known in the art].

8. As per claim 5, Lovett discloses that the pull-down circuit further includes first, second and third transistors [Fig. 14, 18]. Lovett does not disclose all the claimed details. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variation in the circuit design as other components used in the circuit design are well known in the art.

9. As per claims 6 and 15, Wigley et al disclose that the first load position is coupled to the power supply in a first circuit and the second load position is coupled to the power supply in a second circuit that is parallel to the first circuit [inherent to the system as pull-down circuit is utilized to adjust the output voltage; col. 2, lines 40-45; col. 15, line 51-- col. 16, line 4; col. 18, lines 23-26].

10. As per claims 7 and 16, Wigley et al disclose that the power supply includes a negative remote sense input and the first load position includes connectors, is conductively coupled to provide a second voltage to the first input of the pull-down circuit on a first side of the connectors, and is conductively coupled on a second side of the connectors to provide a fourth voltage to the negative remote sense input of the power supply [inherent to the system as pull-down circuit is utilized to adjust the output voltage; col. 2, lines 40-45; col. 15, line 51-- col. 16, line 4; col. 18, lines 23-26].

11. As per claims 8 and 17, Wigley et al disclose that the power supply has a positive terminal and the positive terminal is coupled to the first load position through cables and PCB

layout [inherent to the system as pull-down circuit is utilized to adjust the output voltage; col. 2, lines 40-45; col. 15, line 51-- col. 16, line 4; col. 18, lines 23-26].

12. As per claim 9, Wigley et al disclose that the pull-down circuit further includes first and second operational amplifiers each having an output and positive and negative inputs [inherent to the system as pull-down circuit is utilized to adjust the output voltage; col. 2, lines 40-45; col. 15, line 51-- col. 16, line 4; col. 18, lines 23-26].

13. As per claims 14, Lovett discloses that the pull-down circuit further includes first, second and third transistors [Fig. 14, 18]. Lovett does not disclose all the claimed details. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variation in the circuit design as other components used in the circuit design are well known in the art.

14. As per claim 18, Lovett discloses that the pull-down circuit further includes first, second and third transistors [Fig. 14, 18]. Lovett does not disclose all the claimed details. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a variation in the circuit design as other components used in the circuit design are well known in the art.

15. As per claim 19, Wigley et al disclose that the adjusted parameter is voltage [col. 2, lines 40-45].

16. As per claim 21, Wigley et al disclose that a first conductor coupled between the positive terminal and the first load position; and a second conductor coupled between the positive terminal and the second load position; and wherein a voltage drop of greater than 1% of the voltage between the positive and negative terminals of the power supply exists across both conductors [inherent to the system as pull-down circuit is utilized to adjust the output voltage; col. 2, lines 40-45; col. 15, line 51-- col. 16, line 4; col. 18, lines 23-26].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
December 10, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100